IN THE CLAIMS:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate including an active region and an isolating region provided so as to enclose the active region;

a capacitance insulating film that is provided on the active region and in contact with the isolating region;

an upper electrode provided on the capacitance insulating film so as to be spaced away from the isolating region;

an electrode pad provided on the isolating region;

a lead conductive film provided over a part of the capacitance insulating film and a part of the isolating region for connecting the upper electrode and the electrode pad; and

an interlayer insulating film provided over the substrate,

wherein contact holes penetrating the interlayer insulating film to reach the electrode pad are formed, and

a ratio (S/L) of a total sum of exposed areas S of the electrode pad in the contact holes, with respect to a total sum of widths L of the lead conductive films on the boundary line between the active region and the isolating region, is ~~small enough so that a breakdown ratio of the capacitance insulating film will have no practical problem~~ adjusted such that a breakdown ratio of the capacitance insulating film is substantially 0 during plasma etching for forming the contact holes.

2. (Currently Amended) The semiconductor device according to claim 1, wherein the ~~value~~ ratio (S/L) is 4 or less than 4.

3. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate including an active region and an isolating region formed so as to enclose the active region;

a capacitance insulating film that is formed on the active region and has a boundary portion in contact with the isolating region;

an upper electrode provided on the capacitance insulating film so as to be spaced away from the isolating region;

an electrode pad formed on the isolating region;

a lead conductive film provided over a part of the capacitance insulating film and a part of the isolating region for connecting the upper electrode and the electrode pad; and

an interlayer insulating film provided over the substrate,

wherein contact holes penetrating the interlayer insulating film to reach the electrode pad are formed, [[and]]

the active region in contact with the boundary portion includes a region containing impurities having an oxidation enhanced diffusion effect, and

the capacitance insulating film is formed by oxidizing the active region and has a larger thickness in the boundary portion than in other portions.

4. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate including a first active region an isolating region formed so as to enclose the first active region, and a second active region provided such that the isolating region is sandwiched by the second active region and the first active region;

a first capacitance insulating film that is formed on the first active region and has a boundary portion in contact with the isolating region;

a second capacitance insulating film formed on the second active region;

an upper electrode provided on the first capacitance insulting film so as to be spaced away from the isolating region;

an electrode pad formed on the isolating region;

a lead conductive film provided over a part of the first capacitance insulating film and a part of the isolating region for connecting the upper electrode and the electrode pad; and

an interlayer insulating film provided over the substrate,

wherein first contact holes penetrating the interlayer insulating film to reach the electrode pad and second contact holes penetrating the interlayer insulating film and the second capacitance insulating film to reach the second active region are provided, and

~~a diameter of the second contact hole is larger than that of the first contact hole~~ a total sum of exposed areas of the second active region in the second contact holes is smaller than a total sum of exposed areas of the electrode pad in the first contact holes.

5. (Cancelled).

6. (Currently Amended) The semiconductor device according to claim 4,

wherein ~~an aspect ratio of the first contact hole is equal to that of the second contact hole~~ the quantity of the second contact holes is adjusted such that the total sum of exposed areas of the second active region in the second contact holes is smaller than the total sum of exposed areas of the electrode pad in the first contact holes.

7. (Withdrawn) A method for producing a semiconductor device comprising:

step (a) of preparing a semiconductor substrate including an active region in its upper portion;

step (b) of forming an isolating region in an upper portion of the semiconductor substrate so as to enclose the active region;

step (c) of forming a capacitance insulating film having a boundary portion in contact with the isolating region on the active region;

step (d) of forming an upper electrode provided on the capacitance insulating film so as to be spaced away from the isolating region; an electrode pad formed on the isolating region; and a lead conductive film over a part of the capacitance insulating film and a part of the isolating region for connecting the upper electrode and the electrode pad;

step (e) of forming an interlayer insulating film over the substrate; and

step (f) of forming contact holes penetrating the interlayer insulating film to reach the electrode pad by plasma etching such that a ratio of a total sum of exposed areas of the electrode pad in the contact holes with respect to a total sum of widths of the lead conductive films in the boundary portion is a certain value or less.

8. (Withdrawn) The semiconductor device according to claim 7,

wherein in the step (f), the contact holes are formed such that the ratio is a certain value or less by adjusting the number of the contact holes.

9. (Withdrawn) The semiconductor device according to claim 7,

wherein in the step (f), the contact holes are formed such that the ratio is a certain value or less by adjusting the exposed areas of the electrode pad in the contact holes.

10. (Withdrawn) The semiconductor device according to claim 7,

wherein in the step (f), the contact holes are formed such that the ratio is a certain value or less by adjusting the total sum of the widths of the lead conductive films in the boundary portion.

11. (Withdrawn) The semiconductor device according to claim 7,

wherein in the step (f), the contact holes are formed by adjusting an aspect ratio of the contact holes while satisfying conditions that allow the ratio to be a certain value or less.

12. (Withdrawn) A method for producing a semiconductor device comprising:

step (a) of preparing a semiconductor substrate including an active region;

step (b) of forming an isolating region in an upper portion of the semiconductor substrate;

step (c) of introducing impurities having an oxidation enhanced diffusion effect in a portion bordering the isolating region of the active region;

step (d) of forming a capacitance insulating film having a boundary portion in contact with the isolating region by oxidizing an upper portion of the active region;

step (e) of forming an upper electrode provided on the capacitance insulating film so as to be spaced away from the isolating region, an electrode pad formed on the isolating region, and a lead conductive film over a part of the capacitance insulating film and a part of the isolating region for connecting the upper electrode and the electrode pads;

step (f) of forming an interlayer insulating film over the substrate; and

step (g) of forming contact holes penetrating the interlayer insulating film to reach the electrode pad by plasma etching.

13. (Withdrawn) A method for producing a semiconductor device comprising:

step (a) of preparing a semiconductor substrate including an active region;

step (b) of forming an isolating region in an upper portion of the semiconductor substrate to separate the active region into a first active region and a second active region;

step (c) of forming a first capacitance insulating film having a boundary portion in contact with the isolating region on the first active region, and forming a second capacitance insulating film on the second active region;

step (d) of forming an upper electrode provided on the first capacitance insulating film so as to be spaced away from the isolating region; an electrode pad formed on the isolating region; and a lead conductive film provided over a part of the first capacitance insulating film and a part of the isolating region for connecting the upper electrode and the electrode pads;

step (e) of forming an interlayer insulating film over the substrate; and

step (f) of forming first contact holes penetrating the interlayer insulating film to reach the electrode pads and second contact holes penetrating the interlayer insulating film and the second capacitance insulating film to reach the second active region by plasma etching.

14. (Withdrawn) The method for producing a semiconductor device according to claim 13,

wherein in the step (f), the contact holes are formed such that a diameter of the second contact hole is larger than that of the first contact hole.

15. (Withdrawn) The method for producing a semiconductor device according to claim 14,

wherein in the step (f), the contact holes are formed such that an aspect ratio of the first contact hole is equal to that of the second contact hole.

16. (Previously presented) The semiconductor device according to claim 1,

wherein the widths of the lead conductive films are substantially constant.

17. (New) A semiconductor device comprising:

a semiconductor substrate including an active region and an isolating region having a shallow trench isolation structure formed so as to enclose the active region;

a capacitance insulating film that is formed on the active region and has a boundary portion in contact with the isolating region;

an upper electrode provided on the capacitance insulating film so as to be spaced away from the isolating region;

an electrode pad formed on the isolating region;

a lead conductive film provided over a part of the capacitance insulating film and a part of the isolating region for connecting the upper electrode and the electrode pad; and

an interlayer insulating film provided over the substrate,

wherein contact holes penetrating the interlayer insulating film to reach the electrode pad are formed, and

the capacitance insulating film has a larger thickness in the boundary portion than in other portions.